5

10

15

20



A CMOS logic circuit is disclosed wherein the number of kinds\of basic parts is suppressed to five to allow designing of a circuit which operates at a high speed and repetitiveness of wiring lines is increased to allow designing of \a circuit which is simple in circuit scale and high in expandability and besides the time required for adjustment of components is reduced significantly to reduce the man-hours for arrangement significantly to reduce the man-hours for development significantly and the same basic parts are used so as to achieve augmentation of the yield and promote reduction of the production cost. A basic cell of the CMOS logic circuit includes a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting the inverted signal, a second inversion section for inverting a second input signal having the other of the positive logic and the negative logic and outputting the inverted signal,\and a transmission section for selectively outputting one of the output of the first inversion section and the output of the second inversion section in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal.